Through-Silicon Vias: Drivers, Performance, and Innovations

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(Invited Paper)

Abstract—To address the abating performance improvements from device scaling, innovative 2.5-D and 3-D integrated circuits with vertical interconnects called through-silicon vias (TSVs) have been widely explored. This paper reviews TSVs with focus on the following: 1) key drivers for TSV-based integration; 2) TSV fabrication techniques; 3) TSV electrical and thermomechanical performance fundamentals and characterization techniques; and 4) novel technologies to attain enhanced performance beyond the state-of-the-art TSVs.

Index Terms—Loss, low power, photodefinition, polymer, stress, through-silicon vias (TSVs).

I. INTRODUCTION: DRIVERS

THE integrated circuit (IC), invented in 1958, has been the key technology fueling the information revolution owing to its constant improvements in productivity and performance [1], [2]. Following Moore's [3] projection, the number of transistors per unit area has continually increased with device scaling. This increase in transistor density has been a key factor in reducing gate cost and yielding affordable ICs with more functionality [4]. Moreover, gate speeds have increased by more than $100\times$, and the performance of microprocessor ICs has increased by more than $3000\times$ since the introduction of complementary metal–oxide–semiconductor (MOS) microprocessors [5]. System performance advancements demand higher bandwidth-density off-chip communication with reduced power consumption [6]. However, owing to the slower rate of growth of interconnection and packaging technologies, system performance gains have been abating, thereby creating a critical demand for innovation in silicon ancillary technologies [1].

In addition to attaining high bandwidth density and low-power off-chip communication, the integration of different functionalities, for example, digital, analog, and radio frequency (RF), is highly desired to attain turnkey computing and communication solutions. This need for the integration of different functionalities has led to the development of heterogeneous platforms using system-on-chip architectures [7]; however, there are challenges as described next. Unlike digital circuits, the performance of analog systems can be affected by scaling. For example, scaled MOS transistors degrade matching and noise in analog circuits, while a reduction of the supply voltage affects signal-to-noise ratios [8]. Moreover, with respect to RF systems, technologies, such as III–V heterojunction bipolar transistor-based solutions, may be needed for performance and cost effectiveness of power amplifiers [9]. In addition, there is a need to integrate antennas on a platform with an RFIC to enable phased arrays for millimeter-wave communication [10]. These needs for the integration of different technologies with an optimized technology for each IC necessitate the development of innovative system interconnection platforms.

A. 2.5-D and 3-D Integration Platforms

High bandwidth density, low-power chip-to-chip communication, and heterogeneous integration have been key drivers for innovative system integration technologies. Two such highly explored technologies are 2.5-D and 3-D platforms enabling the integration of a wide range of chip technologies [1], [11]–[13]. In general, 2.5-D integration is defined as the assembly of multiple ICs (in a 2-D plane) over passive interposer substrates, such as silicon (without active devices), glass, or fine-pitch organic substrates [14]–[16]. In addition to passive interposers, active interposers have also been gaining interest recently [17]. Owing to the finer pitch wiring and shorter chip-to-chip distance compared with conventional integration, 2.5-D integration enables high bandwidth density and low-power communication between heterogeneous ICs. Utilizing 2.5-D platforms, a wide range of integration capabilities have been demonstrated in the literature. Field-programmable gate arrays with a digital-to-analog converter integrated on a silicon interposer [12], a millimeter-wave transceiver with a silicon interposer supporting an RFIC and antennas [18], and a heterogeneous integration of a GPS RF receiver chip, a baseband ARM chip, and a DRAM chip on a silicon substrate [19] have been shown in the literature. Moreover, to attain even higher bandwidth density and lower power communication between chips, 3-D integration is highly explored in the literature [1] and is defined as the stacking of layers with active devices (for example, stacking of memory and logic chips or analog and digital chips).
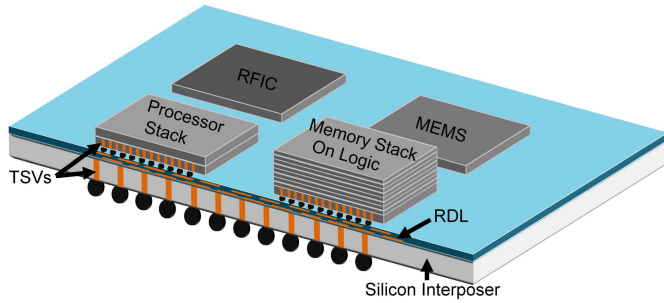
Fig. 1. 3-D system featuring a silicon interposer with TSVs supporting heterogeneous ICs.

B. TSVs as Key Enablers for 2.5-D and 3-D Integration

Vertical interconnections, called through-silicon vias (TSVs), play a key role in enabling 2.5-D and 3-D integration. TSVs consist of metal conductors (commonly copper) insulated from silicon commonly using a thin dielectric liner. Alternative interconnection technologies for stacking include wire bonding, which is electrically inferior and has limited interconnection density compared with TSVs, and proximity communication, such as inductive coupling [20]–[22]. In addition to the TSV-based 3-D integration, monolithic 3-D integration is promising to enable the stacking of transistor layers using monolithic interlayer vias [23], [24]. Moreover, die-to-die interconnection using a silicon bridge has also been shown in the literature [25]; here, no TSVs are needed in the silicon bridges, since they are buried in the organic package. This paper focuses on TSVs for 2.5-D and 3-D ICs, as shown in Fig. 1.

C. TSV Electrical and Thermomechanical Performance

Understanding the electrical and thermomechanical behaviors of TSVs is critical to build 2.5-D and 3-D systems with enhanced performance. For example, for a system with an RFIC and antennas on an interposer, the TSVs need to support the passage of RF signals (with typically less than 0.6-dB insertion loss for 60-GHz applications [26]) from different RF blocks on a circuit board to the IC on the interposer. Consequently, understanding the electrical losses and impedance control of such TSVs is critical, and such an understanding leads to the foundation of novel technology development. Moreover, TSV electrical and thermomechanical performances depend on material properties, dimensions, and geometrical arrangement; poor TSV material choices and designs could affect the system performance. In addition, it is critical to accurately characterize the electrical and thermomechanical performances of TSVs to validate designs, identify bottlenecks, and improve manufacturability.

This paper presents a review of TSV technologies with fabrication and characterization techniques described in Section II. Novel TSV technologies for enhanced performance are described in Section III. In addition to developing high-performance TSV technologies, reliable assembly and efficient cooling (including isolation) are other
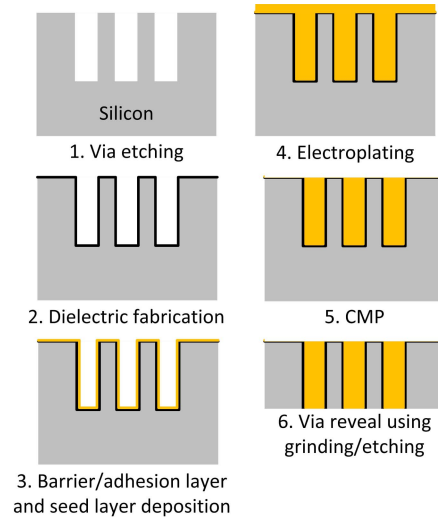

Fig. 2. TSV fabrication flow.

key requirements for 2.5-D and 3-D integration as discussed in the literature [27]–[30].

II. Technology and Performance

This section describes TSV fabrication technologies and explores the fundamentals of TSV electrical and thermomechanical performances along with their characterization techniques.

A. Fabrication Techniques and Specifications

As shown in Fig. 2, the fabrication of TSVs begins with via etching commonly implemented using a Bosch process with alternating etch and passivation cycles [31]. Either blind or through vias may be fabricated. To control critical dimensions during etching, various endpoint detection techniques have been shown in the literature using optical-emission spectroscopy [32], Langmuir probe [33], laser interferometry [34], and RF sensors [35]. Moreover, interferometry-based methods have been implemented for blind vias to control the base critical dimensions of the vias [36]. Once vias are etched, a dielectric deposition or growth is performed yielding a thin (<1 μm) dielectric isolation liner (for example, silicon dioxide). Next, a barrier/adhesion layer is deposited, for example, TaN or TiN [37], followed by seed layer deposition (commonly copper). The barrier/adhesion layer prevents copper diffusion into the silicon substrate and also provides adhesion between the seed layer and the dielectric liner. Once the seed layer is deposited, void-free superfill copper electroplating is performed [38]. Following TSV metallization, chemical-mechanical polishing (CMP) is performed to remove additional metal [39]. Next, in the case of blind vias, the back-side silicon is removed, using either polishing or etching, to expose the TSVs.

The fabrication of TSVs can be performed in different sequences with respect to front-end-of-line (FEOL) transistor fabrication and back-end-of-line (BEOL) metallization. For ICs, the TSV fabrication process is commonly classified into three types: via-first with TSVs fabricated prior to FEOL,

TABLE I

COMPARISON OF TSV FABRICATION METHODS

	Specifications	Via-first [40]–[42]	Via-middle [43], [44]	Via-last [45], [46]	Interposer [12], [47], [48]
1	Process	Before FEOL	After FEOL and before BEOL	After FEOL and BEOL	Commonly before RDL
2	Diameter	1-5 μm	3-6 μm	5-10 μm	10-50 μm
3	Conductor	W and polysilicon	Commonly copper	Copper	Copper
4	Advantages	Thermal oxide growth for liners yielding better isolation	More metallization options compared to via-first	Ease of manufacturing on wafers from different manufacturers	Ease of fabrication
5	Challenges	Limited metallization options and higher resistance	Conformal liners demand deposition of greater thickness	Control of via alignment challenging	Electrical loss

via-middle with TSVs fabricated following FEOL but prior to BEOL, and via-last with TSVs fabricated following FEOL and BEOL either before or after wafer thinning [41], [42]. Since via-first involves TSVs fabricated prior to FEOL, the TSVs must sustain subsequent high-temperature processing steps (~1000 °C) limiting the via metallization options (for example, tungsten and doped polysilicon, which exhibit higher electrical resistivity compared with copper). Compared with via-first, via-middle TSV processing provides greater freedom in the metallization (including copper), since BEOL processing temperatures are commonly less than 400 °C. Moreover, compared with via-first and via-middle, the via-last process can be implemented on a wafer fabricated by other manufacturers [49]. However, TSV alignment to metal pads and FEOL could be challenging when the via-last process is performed from the back side of a thinned bonded wafer. In addition to ICs, the TSVs for interposers can be fabricated before or after metallization and are larger in dimensions. Commonly, the interposer TSVs are fabricated before redistribution layer metallization similar to via-middle TSVs [50]. Table I shows a comparison between the TSV fabrication processes and their specifications.

B. TSV Electrical Fundamentals and Characterization

TSV electrical performance is dependent on various factors, including material, dimensions, arrangement, and frequency of operation. To capture the impact of these factors, resistance, inductance, conductance, and capacitance ($RLGC$) compact physical models have been widely explored in the literature [51]–[56]. Moreover, Pi or T equivalent circuit models using such $RLGC$ models help understand the behavior of TSVs. As shown in Fig. 3, for a signal-ground TSV pair, the TSVs are modeled using resistors and inductors with silicon conductance, and oxide and silicon capacitances between the signal and ground TSVs. For simplicity, the depletion capacitance is neglected (assuming floating silicon). Low-frequency/DC TSV models are demonstrated in the literature [57]. Since it is critical to understand the frequency-dependent behavior of TSVs, this is addressed next using per-unit-length $RLGC$ equations as demonstrated in [51] and [54].
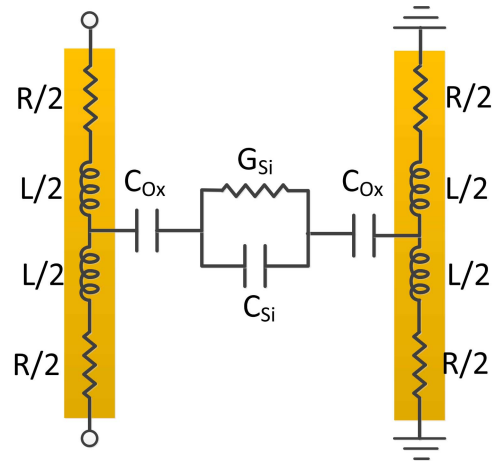

Fig. 3. Signal-ground TSV pair circuit model [51].

The per-unit-length resistance is given by

$$R_u = \sqrt{R_{\text{dc}_{\text{TSV}}}^2 + R_{\text{ac}_{\text{TSV}}}^2}, \tag{1}$$

where

$$R_{\text{dc}_{\text{TSV}}} = \frac{\rho}{\pi r^2};$$

$$R_{\text{ac}_{\text{TSV}}} = (2\pi f \delta)\left(\frac{\mu}{\pi}\right)\left(\frac{p}{2r\sqrt{p^2 - 4r^2}}\right);$$

and

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}}.$$

In Equation (1), ρ is the resistivity of copper, r is the copper via radius, p is the TSV pitch, f is the frequency, μ is the permeability, and δ is the skin depth.

Next, the per-unit-length inductance is given by

$$L_u = \left[\frac{\mu}{\pi}\cosh^{-1}\left(\frac{p}{2r}\right)\right] + \left(\frac{R_u}{2\pi f}\right). \tag{2}$$

Moreover, the models for capacitance and conductance per unit length are shown as follows, where ϵ is the permittivity, t_{oxide} is the thickness of dielectric liner, and σ_{sub} is the substrate conductivity.

First, the per-unit-length oxide capacitance is evaluated as

$$C_{u_{\text{oxide}}} = \frac{2\pi \epsilon_{\text{oxide}}}{\ln\left(\frac{r + t_{\text{oxide}}}{r}\right)}. \tag{3}$$

TABLE II
TSV PERFORMANCE AS A FUNCTION OF DIFFERENT VARIABLES. MI = MINIMAL IMPACT, L = LOW FREQUENCY, AND H = HIGH FREQUENCY

	Increasing	Resistance	Inductance	Capacitance	Conductance	Impedance	Insertion loss
1	Diameter	↓	↓	↑	↑	↓	↓L ↑H
2	Length	↑	↑	↑	↑	MI	↑
3	Pitch	↑	↑	↓	↓	↑	↑L ↓H
4	Silicon conductivity	MI	MI	↑	↑	↓	↑
5	Metal conductivity	↓	↓	MI	MI	↓	↓
6	Liner thickness	MI	MI	↓	↓	↑	↓
7	Frequency	↑	↓	↓	↑	↑L ↓H	↑

Next, the per-unit-length substrate capacitance and conductance between the signal and ground TSVs are evaluated first accounting for the combined contribution of the capacitance and conductance components as

$$C'_{u_{\text{sub}}} = \frac{\pi \epsilon_{\text{sub}}(1 - j(\tan \delta_d + \tan \delta_c))}{\ln\left(\frac{p}{2(r+t_{\text{oxide}})} + \sqrt{\left(\frac{p}{2(r+t_{\text{oxide}})}\right)^2 - 1}\right)} \quad (4)$$

where $\tan \delta_d$ represents the polarization losses of silicon and can be considered zero for the TSVs with silicon dioxide liner [51]. Moreover, $\tan \delta_c$ represents losses as a result of the conductivity of silicon where

$$\tan \delta_c = \frac{1}{\omega \epsilon_{\text{sub}} \rho_{\text{Si}}}. \quad (5)$$

Next, the combined capacitance and the conductance component of the TSVs with silicon dioxide liner is given by

$$C_{u_{\text{Total}}} = \frac{1}{\frac{1}{C_{u_{\text{oxide}}}} + \frac{1}{C'_{u_{\text{sub}}}} + \frac{1}{C_{u_{\text{oxide}}}}}. \quad (6)$$

From the calculated $C_{u_{\text{Total}}}$, the TSV capacitance and the conductance are extracted as follows:

$$C_u = \text{Re}(C_{u_{\text{Total}}}) \quad (7)$$

and

$$G_u = -\omega \text{Im}(C_{u_{\text{Total}}}). \quad (8)$$

Using the $RLGC$ values, impedance and insertion loss can be extracted. Next, considering the models, the impact of increasing radius, length, pitch, silicon conductivity, metal conductivity, liner thickness and frequency on $RLGC$, impedance, and insertion loss are shown in Table II. The impact on insertion loss is considered accounting frequency [62], since TSV behavior is frequency dependent with four distinct regions [51]: slow-wave, transition, dielectric quasi-TEM, and skin effect. At low frequencies, the effects of R, L, and C_{oxide} on the loss are greater, since the slow-wave mode electrically shields the silicon substrate. At higher frequencies, the impact of substrate capacitance and conductance is greater due to higher losses in silicon. Moreover, with respect to the TSV capacitance, as the frequency increases, the capacitance reduces due to transition from the slow-wave mode to the dielectric quasi-TEM mode when the frequency

is higher than the relaxation frequency of the silicon substrate (silicon acts as a dielectric) [51], [63].

In addition to understanding TSV electrical performance using compact physical models, TSV characterization is critical to validate models and simulations. At DC frequencies, the four-point resistance measurement method can accurately measure TSV resistance, and TSV-to-silicon leakage measurements can provide insight into the quality of a dielectric isolation layer. The commonly measured TSV DC resistance values are in the range of 20–100 mΩ, and the TSV leakage values before failure are <1 nA [57], [69], [70]. Moreover, at low frequencies, capacitance can be measured using impedance-based measurement techniques [69], [71]. For capacitance measurements, relatively large capacitance values are needed to measure above a tool's resolution requiring bundling of TSVs with all the TSVs electrically connected to a metal probing pad and the silicon around each TSV electrically grounded using ohmic rings around each TSV [69]. Consequently, de-embedding is needed and implemented in the literature by subtracting the capacitance of horizontal wires from the total capacitance. Dividing the result by the number of TSVs yields the capacitance per TSV commonly measured close to 100 fF [69], [70]. Last, for higher frequencies, two-port and one-port measurements have been explored in the literature [26], [58], [63], [72]–[74]. With TSV high-frequency measurements, de-embedding is critical to understand the loss of TSVs and has been demonstrated in the literature using techniques, such as L-2L, Thru-Reflect-Line (TRL), two-port open-short, and one-port open-short [58]–[61], as explained in Table III. Next, the $RLGC$ values of TSVs can be extracted from the de-embedded TSVs using either Y or Z parameters or using transmission-line-based extraction techniques [54], [63].

Moreover, along with understanding the electrical performance of TSVs, it is critical to understand the interactions between TSVs, as well as TSVs and active devices. The coupling between TSVs is dependent on the capacitance and conductance dominated impedance and losses between the TSVs; the impedance and the losses depend on liner thickness, silicon conductivity, and TSV pitch [75]. The impact of TSV-to-TSV coupling can be reduced using ground shielding TSVs between signal TSVs [12]. Moreover, the TSV-to-device coupling defines a keep out zone (KOZ) for devices and needs to be considered during TSV placement. With respect

TABLE III

COMPARISON OF TSV DE-EMBEDDING TECHNIQUES IN THE LITERATURE

	Techniques	Principle	Benefit	Limitation
1	**TRL [58]**	Second and third tier TRL implementation	Accurate de-embedding demonstrated up to 60 GHz	Difficulty in obtaining reference impedances for 3D transitions
2	**Single-port [59]**	Open and short structures for $RLGC$ extraction	Simpler fabrication for $RLGC$ extraction	Difficult to obtain accurate opens and shorts at higher frequencies
3	**L-2L [60]**	TSV-trace-TSV links with different trace lengths	Simpler TSV loss extraction structures	Demonstrated in the literature up to 50 GHz; application at higher frequencies unknown
4	**Open-short [61]**	Open-short structures with $ABCD$ matrices to extract TSV loss	Simpler TSV loss extraction structures	Difficult to obtain accurate opens and shorts at higher frequencies

to immunity for TSV-to-device coupling, FinFETs have been shown to have superior performance compared with planar MOSFETs due to only capacitive coupling being dominant in the ON-state compared with noise amplification through the bulk transconductance for planar MOSFETs [76]. To reduce TSV-to-device coupling, the use of a guard ring around TSVs may help [75].

Equipped with understanding of TSV fabrication techniques and electrical performance, the next critical factor reviewed is thermomechanical reliability fundamentals and characterization.

C. TSV Thermomechanical Fundamentals and Characterization

Since copper expands significantly more than silicon when a thermal load is applied, TSVs exhibit a unique thermomechanical behavior that may lead to a potential impact on nearby devices increasing TSV KOZ, cohesive cracks in copper, cohesive cracks in silicon, and adhesive delamination of copper vias [77], [78]. Moreover, protrusion of copper vias called copper pumping has been shown to damage BEOL structures [79].

To understand TSV stresses, various models have been shown in the literature using finite element modeling [80], [81]. Using a simpler 2-D plane-strain analytical model (Lamé stress solution), thermal stresses near an infinitely long TSV embedded in an unbound matrix can be expressed as [82]

$$\sigma_{rr}^m = -\sigma_{\theta\theta}^m = -\frac{B \triangle\alpha\triangle T}{2}\left(\frac{R}{r}\right)^2 \qquad (9)$$

and

$$\sigma_{zz}^m = \sigma_{rz}^m = \sigma_{\theta z}^m = \sigma_{r\theta}^m = 0 \qquad (10)$$

where m refers to the matrix, B is the biaxial modulus, $\triangle\alpha$ is the coefficient of thermal expansion (CTE) mismatch, $\triangle T$ is the differential thermal load, R is the TSV radius, and r is the distance from the TSV center. Equation (9) shows TSV stresses are higher for larger diameter TSVs and reduce as the distance increases from the TSVs.

Moreover, in addition to TSV dimensions, the TSV stresses also depend on thermal history and copper microstructure affecting the copper plasticity, and thus, these factors must be carefully considered while designing TSVs [83].

With respect to evaluating the impact of TSV stress and estimating KOZ, models have been shown in the literature [84]. In addition, with matured TSV manufacturing techniques and reduction in TSV diameters, ICs with minimal impact on the device performance due to the presence of TSVs have been demonstrated in the literature [85]. Moreover, with respect to copper pumping, pre-CMP anneal and copper microstructure control techniques have been demonstrated in the literature to control TSV protrusions and, thereby, improve reliability [86]–[88]. While the TSV pumping challenge has been addressed by pre-CMP anneal and microstructure control, the annealing process yields silicon with tensile strains. To address this challenge, a CMP stop layer optimization technique has been demonstrated using a CMP stop layer with $4\times$ CTE and one third elasticity modulus [89]. Owing to the CTE and elasticity modulus properties, the CMP stop layer shrinks following pre-CMP anneal and results in compressive strains in the silicon balancing the tensile strains. Consequently, the CMP stop layer optimization technique reduces TSV KOZ significantly. Lastly, with respect to structural failures, TSV cracks can result after thermal cycling demanding novel solutions to reduce TSV stress [78]. With improved manufacturing and designs, TSVs have been demonstrated without failures up to 1000 thermal cycles based on the JEDEC standards [90].

In addition to understanding TSV thermomechanical behavior using modeling and simulations, it is critical to characterize stresses in standalone and stacked ICs with TSVs to prove their reliability. Efforts in TSV stress/strain measurements for TSV reliability exploration include micro-Raman spectroscopy [64], [65], bending beam technique [66], indentation [67], and synchrotron x-ray diffraction (XRD) [91], as shown in Table IV. In comparison, synchrotron XRD seems promising, since it can measure all the stress components in a copper via and the surrounding silicon with minimal destruction to the TSV sample. Synchrotron XRD strain measurements for standalone wafers with different types of TSVs

TABLE IV
COMPARISON OF TSV STRESS MEASUREMENT TECHNIQUES IN THE LITERATURE

|	Techniques	Principle	Benefit	Limitation
1	Micro-Raman spectroscopy [64], [65]	Frequency shift measurement of an impinging laser	Localized near surface Si stress measurement	Stress in copper cannot be measured
2	Bending beam technique [66]	Curvature measurement	Stress measurement in Si and Cu	Averaged stresses obtained
3	Indentation [67]	Residual-stress-induced normal load measurement	Stress measurement in Si and Cu	Requires a known stress-free state
4	Synchrotron XRD [68]	Raster scanning under a micro focused x-ray beam	Stress measurement in Si and Cu with minimum destruction	Challenging data interpretation
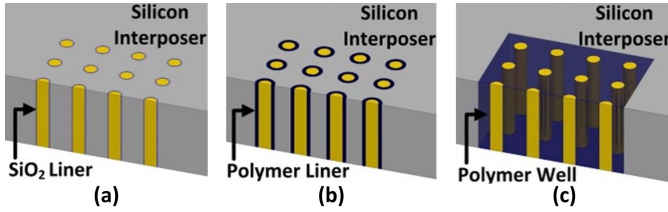
Fig. 4. Schematics of (a) TSVs with silicon dioxide liner, (b) polymer-clad TSVs, and (c) polymer-embedded vias.

and data interpretation using beam-intensity-based method have been demonstrated in [92]. Moreover, synchrotron XRD strain measurements for stacked ICs with TSVs have also been shown in the literature [93].

III. INNOVATIONS

To attain a significant reduction in TSV stress and electrical loss, this section describes select innovations in TSVs with the main focus being on polymer-enhanced TSVs. The polymer-enhanced TSVs in this section include polymer-clad TSVs with thick polymer liners, polymer-embedded vias with copper vias embedded in polymer wells within silicon, and coaxial configurations of the polymer-embedded vias [94], [95]. Fig. 4 shows the structures of the polymer-enhanced TSVs in comparison with the conventional TSVs.

A. Polymer-Clad TSVs

To reduce TSV stress and capacitance, various liner techniques have been explored in the literature, including air and thick polymer. Compared with silicon dioxide liner, air liners with a lower relative dielectric constant and thick polymer liners can reduce TSV stress and liner capacitance. Moreover, owing to the liner capacitance reduction, the air and thick polymer liners also reduce the impact of slow-wave mode lowering electrical losses [96].

Thick ($\sim$30 μm) air liners can be fabricated by etching silicon around the fabricated TSVs [97], whereas thin ($\sim$3 μm) air liners can be fabricated by depositing a dielectric layer over circular trenches in silicon until the trenches get pinched off or alternatively by using a sacrificial material filled in the circular trenches [98] followed by TSV fabrication at the center of the trenches [99]. Moreover, TSVs with air isolation can be

obtained by etching silicon up to a specific depth around the TSVs [100].

Compared with the air liners, the main advantage of using polymer liners is that the fabrication of horizontal interconnects is easier over polymer liners than air liners. With respect to TSV stress, various modeling results have shown the reduction of stress for TSVs with thick polymer liners. Using a 5-μm thick benzocyclobutene (BCB) stress buffer layer for 30-μm diameter vias, Ryu et al. [101] have shown a significant reduction in radial and shear stress along Cu/BCB and BCB/Si interfaces compared with Cu/Si interface. Using Parylene as a liner, Chen et al. [102] have shown that normal stresses in copper, dielectric, and silicon are lower for the TSVs with a Parylene liner compared with the TSVs with silicon dioxide liner; when the Parylene thickness is increased from 1 to 15 μm, the normal stresses in copper, dielectric, and silicon are reduced by half. In addition to modeling, thermomechanical characterization of polymer-clad TSVs and comparison with the TSVs with silicon dioxide liner has been demonstrated in [103] using synchrotron XRD showing a 30% reduction in TSV strains at the liner–silicon interface. Moreover, with respect to TSV capacitance, Thadesar and Bakir [104] have shown using modeling that the TSV dielectric capacitance can be reduced from 3.515 to 0.165 pF using 20-μm-thick SU-8 liners compared with 1-μm-thick silicon dioxide liners for 400-μm tall and 80-μm diameter copper vias.

The fabrication of polymer liners has been described in the literature using polymer vapor deposition [107], polymer filling in circular trenches within silicon [108], photodefinition of polymer-filled vias with a temporary release film to fabricate coaxial TSVs [109], laser ablation of polymer-filled vias [110], and photodefined polymer with a perforated dielectric layer, called mesh layer, at the base [94]. By comparison, the polymer liner formation process using photodefined polymer is simpler. Fig. 5 shows 390-μm tall copper TSVs with $\sim$80 μm diameter and surrounded by a $\sim$20-μm-thick photodefined polymer cladding on a 250-μm pitch.

B. Polymer-Embedded Vias

To achieve further electrical performance enhancement compared with polymer-clad TSVs, polymer-embedded vias are explored for silicon interposers as described next.

High-resistivity silicon interposers can achieve a reduction in TSV losses. However, high-resistivity silicon is

TABLE V
COMPARISON OF POLYMER-EMBEDDED VIAS AND POLYMER-CLAD TSVS WITH OTHER TSV TECHNOLOGIES

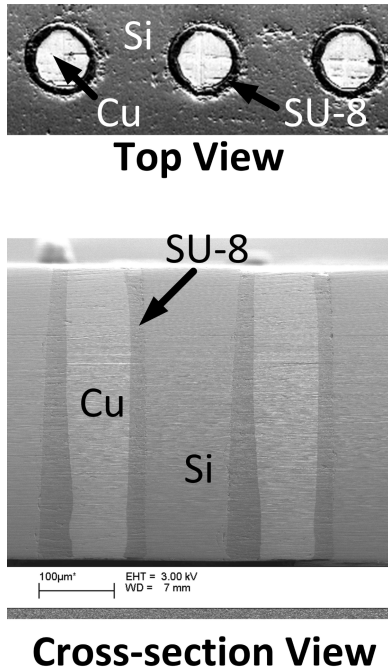| No.	Parameters	Polymer-embedded vias [105]	Polymer-clad TSVs [94]	SiO_2 liner TSVs	Air liner TSVs [98]	Glass Vias [106]
1	Copper via diameter	100/65 μm	80 μm	$\sim$10 μm	20 μm	15 μm at top
2	TSV height	270/370 μm	390 μm	100 μm	65 μm	30 μm
3	TSV pitch	250/150 μm	250 μm	40 μm min.	50 μm	27 μm
4	Loss at high frequency	$\sim$0.2 dB at 30 GHz (thick interposer)	Low	$\sim$1.2 dB at 29 GHz (for a chain with 2 TSVs) [50]	Low	$\sim$0.1 dB at 20 GHz (thin glass for a chain with 2 vias)
5	Ease of fabrication	High	High	Very high	Low	Moderate
6	Special features	Photodefinition	Photodefinition	Simpler fabrication	Metallization over air liners	Panel-scale fabrication

Top View

Cross-section View

Fig. 5.   Polymer-clad TSVs with a thick SU-8 liner [94].
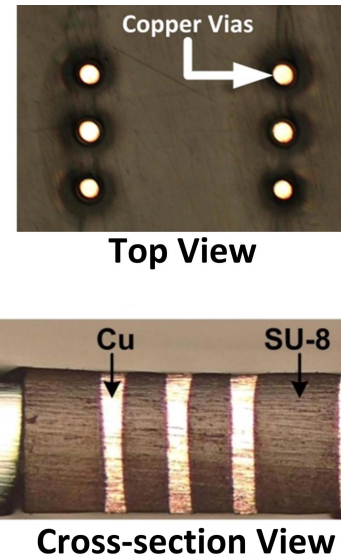

Top View

Cross-section View

Fig. 6.   Polymer-embedded vias with copper vias in SU-8 wells within silicon [112].

A comparison of polymer-embedded vias and polymer-clad TSVs to different TSV technologies in the literature is shown in Table V.

C. Coaxial TSVs

A coaxial interconnect configuration of polymer-embedded vias can be formed by placing ground vias around a signal via [105]. The technique of forming coaxial vias using ground vias is easier to implement compared with other coaxial via techniques in the literature [73], [109], [115] and, consequently, is addressed here.

The coaxial configuration can reduce TSV loss and coupling in addition to providing an impedance-matched interconnection. Fig. 7 shows the fabricated 285-μm tall polymer-enhanced coaxial vias within a 1800 μm $\times$ 1800 μm well in silicon prior to the top layer metallization. The copper via diameter is 65 μm and the signal-to-ground via pitch is 125 μm. To better compare coaxial vias in the literature, a comparison is shown in Table VI. Moreover, RF measurements were performed on open and short measurement structures of the coaxial vias with 150-μm signal-to-ground

expensive [51], [111], and thus, there has been an effort to explore glass interposers [106]. However, glass requires serial ablation to form vias and is a poor thermal conductor compared with silicon. In comparison, polymer-embedded vias consist of copper vias embedded in photodefined polymer wells within the commonly implemented 10-Ω-cm resistivity silicon, thereby providing a wafer-scale batch fabrication solution attaining vias in low-loss regions within an economical silicon [112]. Fig. 6 shows 65-μm diameter and 370-μm tall polymer-embedded vias on a 150-μm pitch within a 1800 μm $\times$ 1800 μm well in silicon.

Similar to polymer-embedded vias, copper vias in dielectric regions within silicon have been demonstrated in the literature using: 1) a metal coating over silicon pillars in polymer wells [113] and 2) glass reflow over etched areas in silicon followed by silicon pillar etching [114]. Compared with these processes, photodefined polymer-embedded vias provide low-loss TSVs with a simpler fabrication process.

TABLE VI

COMPARISON OF THE DEMONSTRATED COAXIAL VIAS TO OTHER COAXIAL TSV TECHNOLOGIES FROM THE LITERATURE

| No.	Parameters	Photodefined coax TSVs with ground shield vias [105]	SiO_2 liner TSVs	Laser ablated annular coax [115]	Laser ablated coax [73]	Photodefined coax [109]
1	Copper via diameter	65 μm	∼10 μm	42 μm	70 μm	100 μm
2	TSV height	285 μm	100 μm	205 μm	150 μm	300 μm
3	TSV pitch	150/125/95 μm	40 μm min.	450 μm	Surrounded by non-coax	500 μm
4	Insertion loss at high frequency	0.1 dB at 50 GHz (for one coaxial TSV)	∼1.2 dB at 29 GHz (for a chain with 2 TSVs) [50]	∼5.5 dB at 20 GHz (for a chain with 4 TSVs)	0.044 dB at 10 GHz (for one coaxial TSV)	∼0.25 dB at 10 GHz (for a TSV-trace link)
5	Ease of fabrication	High	Very high	Moderate	Moderate	Moderate
6	Special features	Photodefinition	Simpler fabrication	Laminated ABF with laser ablation	Coax and non-coax in parallel	Photodefinition
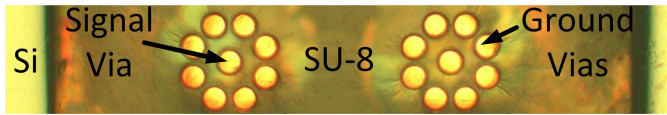
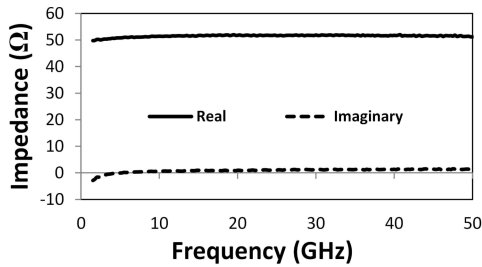Fig. 7.   Polymer-embedded coaxial TSVs with ground shield vias [105].

Fig. 8.   Impedance extraction from measurements of polymer-embedded coaxial TSVs with ground vias [95].

via pitch yielding a wideband impedance match to 50 Ω, as shown in Fig. 8.

IV. CONCLUSION

Key drivers leading to the development of TSV-based integration techniques are discussed along with TSV fabrication technologies. Moreover, TSV electrical and thermomechanical behaviors are described along with measurement techniques for TSV characterization. Last, novel techniques, including polymer-clad TSVs, polymer-embedded vias, and coaxial vias, are demonstrated to attain enhanced TSV performance.

REFERENCES

[1] M. S. Bakir and J. D. Meindl, Eds., *Integrated Interconnect Technologies for 3D Nanoelectronic Systems*. Norwood, MA, USA: Artech House, 2009.

[2] K. Kim, "Silicon technologies and solutions for the data-driven world," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2015, pp. 1–7.

[3] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, no. 8, pp. 114–117, Apr. 1965.

[4] J. Meindl, A. Naeemi, M. Bakir, and R. Murali, "Nanoelectronics in retrospect, prospect and principle," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2010, pp. 31–35.

[5] M. Horowitz, "Computing's energy problem (and what we can do about it)," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2014, pp. 10–14.

[6] K. A. Bowman, A. R. Alameldeen, S. T. Srinivasan, and C. B. Wilkerson, "Impact of die-to-die and within-die parameter variations on the clock frequency and throughput of multi-core processors," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 17, no. 12, pp. 1679–1690, Dec. 2009.

[7] *International Technology Roadmap for Semiconductors (ITRS), Radio-Frequency and Analog/Mixed Signal Technologies for Communications*, 2011.

[8] B. C. Lim, J. Mao, M. Horowitz, J.-E. Jang, and J. Kim, "Digital analog design: Enabling mixed-signal system validation," *IEEE Des. Test*, vol. 32, no. 1, pp. 44–52, Feb. 2015.

[9] S. Kousai, K. Onizuka, S. Hu, H. Wang, and A. Hajimiri, "A new wave of CMOS power amplifier innovations: Fusing digital and analog techniques with large signal RF operations," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2014, pp. 1–8.

[10] X. Gu, A. Valdes-Garcia, A. Natarajan, B. Sadhu, D. Liu, and S. K. Reynolds, "W-band scalable phased arrays for imaging and communications," *IEEE Commun. Mag.*, vol. 53, no. 4, pp. 196–204, Apr. 2015.

[11] J. U. Knickerbocker *et al.*, "System-on-package (SOP) technology, characterization and applications," in *Proc. 56th IEEE Electron. Compon. Technol. Conf. (ECTC)*, May 2006, pp. 415–421.

[12] C. Erdmann *et al.*, "A heterogeneous 3D-IC consisting of two 28 nm FPGA die and 32 reconfigurable high-performance data converters," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 258–269, Jan. 2015.

[13] W. S. Liao *et al.*, "A high-performance low-cost chip-on-wafer package with sub-μm pitch Cu RDL," in *IEEE Symp. VLSI Technol. Dig. Tech. Papers*, Jun. 2014, pp. 1–2.

[14] B. Banijamali, S. Ramalingam, H. Liu, and M. Kim, "Outstanding and innovative reliability study of 3D TSV interposer and fine pitch solder micro-bumps," in *Proc. IEEE 62nd Electron. Compon. Technol. Conf. (ECTC)*, May/Jun. 2012, pp. 309–314.

[15] B. Sawyer *et al.*, "Modeling, design, fabrication and characterization of first large 2.5D glass interposer as a superior alternative to silicon and organic interposers at 50 micron bump pitch," in *Proc. IEEE 64th Electron. Compon. Technol. Conf. (ECTC)*, May 2014, pp. 742–747.

[16] K. Oi *et al.*, "Development of new 2.5D package with novel integrated organic interposer substrate with ultra-fine wiring and high density bumps," in *Proc. IEEE 64th Electron. Compon. Technol. Conf. (ECTC)*, May 2014, pp. 348–353.

[17] G. Hellings *et al.*, "Active-lite interposer for 2.5 & 3D integration," in *IEEE Symp. VLSI Technol. Dig. Tech. Papers (VLSI Technology)*, Jun. 2015, pp. T222–T223.

[18] O. El Bouayadi *et al.*, "Silicon interposer: A versatile platform towards full-3D integration of wireless systems at millimeter-wave frequencies," in *Proc. IEEE 65th Electron. Compon. Technol. Conf. (ECTC)*, May 2015, pp. 973–980.

[19] W. S. Liao *et al.*, "3D IC heterogeneous integration of GPS RF receiver, baseband, and DRAM on CoWoS with system BIST solution," in *IEEE Symp. VLSI Technol. Dig. Tech. Papers*, Jun. 2013, pp. C18–C19.

[20] F. Carson, H. T. Lee, J. H. Yee, J. Punzalan, and E. Fontanilla, "Die to die copper wire bonding enabling low cost 3D packaging," in *Proc. IEEE 61st Electron. Compon. Technol. Conf. (ECTC)*, May/Jun. 2011, pp. 1502–1507.

[21] H. Ishikuro and T. Kuroda, "Wireless proximity interfaces with a pulse-based inductive coupling technique," *IEEE Commun. Mag.*, vol. 48, no. 10, pp. 192–199, Oct. 2010.

[22] Y. Take, H. Matsutani, D. Sasaki, M. Koibuchi, T. Kuroda, and H. Amano, "3D NoC with inductive-coupling links for building-block SiPs," *IEEE Trans. Comput.*, vol. 63, no. 3, pp. 748–763, Mar. 2014.

[23] P. Batude *et al.*, "3D sequential integration opportunities and technology optimization," in *Proc. IEEE Int. Interconnect Technol. Conf., Adv. Metallization Conf. (IITC/AMC)*, May 2014, pp. 373–376.

[24] D. H. Kim and S. K. Lim, "Physical design and CAD tools for 3-D integrated circuits: Challenges and opportunities," *IEEE Des. Test*, vol. 32, no. 4, pp. 8–22, Aug. 2015.

[25] H. Braunisch, A. Aleksov, S. Lotz, and J. Swan, "High-speed performance of silicon bridge die-to-die interconnects," in *Proc. IEEE 20th Conf. Elect. Perform. Electron. Packag. Syst. (EPEPS)*, Oct. 2011, pp. 95–98.

[26] Y. Lamy *et al.*, "A compact 3D silicon interposer package with integrated antenna for 60 GHz wireless applications," in *Proc. IEEE Int. 3D Syst. Integr. Conf. (3DIC)*, Oct. 2013, pp. 1–6.

[27] H. S. Yang, C. Zhang, and M. S. Bakir, "Self-aligned silicon interposer tiles and silicon bridges using positive self-alignment structures and rematable mechanically flexible interconnects," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 4, no. 11, pp. 1760–1768, Nov. 2014.

[28] L. Zheng, Y. Zhang, G. Huang, and M. S. Bakir, "Novel electrical and fluidic microbumps for silicon interposer and 3-D ICs," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 4, no. 5, pp. 777–785, May 2014.

[29] Y. Zhang, Y. Zhang, and M. S. Bakir, "Thermal design and constraints for heterogeneous integrated chip stacks and isolation technology using air gap and thermal bridge," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 4, no. 12, pp. 1914–1924, Dec. 2014.

[30] Y. Zhang, Y. Zhang, T. Sarvey, C. Zhang, M. Zia, and M. Bakir, "Thermal isolation using air gap and mechanically flexible interconnects for heterogeneous 3-D ICs," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 6, no. 1, pp. 31–39, Jan. 2016.

[31] B. Wu, A. Kumar, and S. Pamarthy, "High aspect ratio silicon etch: A review," *J. Appl. Phys.*, vol. 108, no. 5, pp. 051101-1–051101-20, Sep. 2010.

[32] J. M. Gu, P. A. Thadesar, A. Dembla, M. S. Bakir, G. S. May, and S. J. Hong, "Endpoint detection in low open area TSV fabrication using optical emission spectroscopy," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 4, no. 7, pp. 1251–1260, Jul. 2014.

[33] R. M. de Castro *et al.*, "End-point detection of polymer etching using Langmuir probes," *IEEE Trans. Plasma Sci.*, vol. 28, no. 3, pp. 1043–1049, Jun. 2000.

[34] W. Wei, L. Zhongwen, W. Wu, and G. Yungui, "Optical interferometry endpoint detection for plasma etching," in *Proc. 8th Int. Conf. Electron. Meas. Instrum. (ICEMI)*, Aug./Jul. 2007, pp. 4-252–4-255.

[35] H. Handa *et al.*, "Process monitoring of chrome dry-etching with RF sensor for reticle production beyond 90-nm node," *Proc. SPIE*, vol. 5256, pp. 85–92, Dec. 2003.

[36] P. Timoney *et al.*, "New interferometric measurement technique for small diameter TSV," in *Proc. 25th Annu. SEMI Adv. Semiconductor Manuf. Conf. (ASMC)*, May 2014, pp. 37–41.

[37] F. Battegay and M. Fourel, "Barrier material selection for TSV last, flipchip & 3D–UBM & RDL integrations," in *Proc. 65th IEEE Electron. Compon. Technol. Conf. (ECTC)*, May 2015, pp. 1183–1192.

[38] X. Chen, G. Xu, and L. Luo, "Development of seed layer deposition and fast copper electroplating into deep microvias for three-dimensional integration," *IET Micro Nano Lett.*, vol. 8, no. 4, pp. 191–192, Apr. 2013.

[39] J. C. Chen *et al.*, "Impact of slurry in Cu CMP (chemical mechanical polishing) on Cu topography of through silicon vias (TSVs), re-distribution layers, and Cu exposure," in *Proc. 61st IEEE Electron. Compon. Technol. Conf. (ECTC)*, May/Jun. 2011, pp. 1389–1394.

[40] C. Laviron *et al.*, "Via first approach optimisation for through silicon via applications," in *Proc. 59th IEEE Electron. Compon. Technol. Conf. (ECTC)*, May 2009, pp. 14–19.

[41] S. Qu and Y. Liu, *Wafer-Level Chip-Scale Packaging: Analog and Power Semiconductor Applications*. New York, NY, USA: Springer, Sep. 2014.

[42] R. Sharma, *Design of 3D Integrated Circuits and Systems*. Boca Raton, FL, USA: CRC Press, Nov. 2014.

[43] A. Redolfi *et al.*, "Implementation of an industry compliant, 5×50 μm, via-middle TSV technology on 300 mm wafers," in *Proc. 61st IEEE Electron. Compon. Technol. Conf. (ECTC)*, May/Jun. 2011, pp. 1384–1388.

[44] S. Van Huylenbroeck *et al.*, "Advanced metallization scheme for 3×50 μm via middle TSV and beyond," in *Proc. 65th IEEE Electron. Compon. Technol. Conf. (ECTC)*, May 2015, pp. 66–72.

[45] M. Aoki *et al.*, "Fabricating 3D integrated CMOS devices by using wafer stacking and via-last TSV technologies," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2013, pp. 29.5.1–29.5.4.

[46] W. Lin *et al.*, "Prototype of multi-stacked memory wafers using low-temperature oxide bonding and ultra-fine-dimension copper through-silicon via interconnects," in *Proc. IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conf. (S3S)*, Oct. 2014, pp. 1–3.

[47] I. Shubin *et al.*, "Package demonstration of an interposer with integrated TSVs and flexible compliant interconnects," in *Proc. 63rd IEEE Electron. Compon. Technol. Conf. (ECTC)*, May 2013, pp. 329–333.

[48] M. Detalle *et al.*, "Minimizing interposer warpage by process control and design optimization," in *Proc. 64th IEEE Electron. Compon. Technol. Conf. (ECTC)*, May 2014, pp. 33–40.

[49] K. Takeda and M. Aoki, "3D integration technology using hybrid wafer bonding and via-last TSV process," in *Proc. IEEE Int. Interconnect Technol. Conf. (IITC)*, May 2014, pp. 211–214.

[50] N. Kim, D. Wu, D. Kim, A. Rahman, and P. Wu, "Interposer design optimization for high frequency signal transmission in passive and active interposer using through silicon via (TSV)," in *Proc. 61st IEEE Electron. Compon. Technol. Conf. (ECTC)*, May/Jun. 2011, pp. 1160–1167.

[51] I. Ndip *et al.*, "High-frequency modeling of TSVs for 3-D chip integration and silicon interposers considering skin-effect, dielectric quasi-TEM and slow-wave modes," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 1, no. 10, pp. 1627–1641, Oct. 2011.

[52] R. Gordin *et al.*, "Design and modeling methodology of vertical interconnects for 3DI applications," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 1, no. 2, pp. 163–167, Feb. 2011.

[53] E.-X. Liu, E.-P. Li, W.-B. Ewe, H. M. Lee, T. G. Lim, and S. Gao, "Compact wideband equivalent-circuit model for electrical modeling of through-silicon via," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 6, pp. 1454–1460, Jun. 2011.

[54] Z. Xu and J.-Q. Lu, "Through-silicon-via fabrication technologies, passives extraction, and electrical modeling for 3-D integration/packaging," *IEEE Trans. Semicond. Manuf.*, vol. 26, no. 1, pp. 23–34, Feb. 2013.

[55] I. Ndip *et al.*, "Analytical, numerical-, and measurement-based methods for extracting the electrical parameters of through silicon vias (TSVs)," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 4, no. 3, pp. 504–515, Mar. 2014.

[56] R. Wang, G. Charles, and P. Franzon, "Modeling and compare of through-silicon-via (TSV) in high frequency," in *Proc. IEEE Int. Conf. 3D Syst. Integr. (3DIC)*, Jan./Feb. 2012, pp. 1–6.

[57] G. Katti, M. Stucchi, K. De Meyer, and W. Dehaene, "Electrical modeling and characterization of through silicon via for three-dimensional ICs," *IEEE Trans. Electron Devices*, vol. 57, no. 1, pp. 256–262, Jan. 2010.

[58] M. Wojnowski, G. Sommer, A. Klumpp, and W. Weber, "Electrical characterization of 3D interconnection structures up to millimeter wave frequencies," in *Proc. 10th IEEE Electron. Packag. Technol. Conf. (EPTC)*, Dec. 2008, pp. 1393–1402.

[59] C.-W. Luo, Y.-C. Wu, J.-Y. Wang, and S. S. H. Hsu, "RF modeling of through silicon vias (TSVs) in 3D IC," in *Proc. Int. Conf. Solid State Devices Mater.*, 2010, pp. 239–240.

[60] H.-T. Yen *et al.*, "TSV RF de-embedding method and modeling for 3DIC," in *Proc. 23rd Annu. SEMI Adv. Semiconductor Manuf. Conf. (ASMC)*, May 2012, pp. 394–397.

[61] Y.-C. Chang, D.-C. Chang, S. S. H. Hsu, J.-H. Lee, S.-G. Lin, and Y.-Z. Juang, "A matrix-computation based methodology for extracting the S-parameters of interconnects in advanced packaging technologies," in *Proc. IEEE Asia-Pacific Microw. Conf. (APMC)*, Dec. 2011, pp. 1909–1912.

[62] J. Kim *et al.*, "High-frequency scalable electrical model and analysis of a through silicon via (TSV)," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 1, no. 2, pp. 181–195, Feb. 2011.

[63] F. Liu *et al.*, "Electrical characterization of 3D through-silicon-vias," in *Proc. 60th IEEE Electron. Compon. Technol. Conf. (ECTC)*, Jun. 2010, pp. 1100–1105.

[64] S.-K. Ryu *et al.*, "Micro-Raman spectroscopy and analysis of near-surface stresses in silicon around through-silicon vias for three-dimensional interconnects," *J. Appl. Phys.*, vol. 111, no. 6, pp. 063513-1–063513-8, Mar. 2012.

[65] I. De Wolf, V. Simons, V. Cherman, R. Labie, B. Vandevelde, and E. Beyne, "In-depth Raman spectroscopy analysis of various parameters affecting the mechanical stress near the surface and bulk of Cu-TSVs," in *Proc. 62nd IEEE Electron. Compon. Technol. Conf. (ECTC)*, May/Jun. 2012, pp. 331–337.

[66] S.-K. Ryu *et al.*, "Characterization of thermal stresses in through-silicon vias for three-dimensional interconnects by bending beam technique," *Appl. Phys. Lett.*, vol. 100, no. 4, pp. 041901-1–041901-4, Jan. 2012.

[67] G. Lee, M.-J. Choi, S.-W. Jeon, K.-Y. Byun, and D. Kwon, "Microstructure and stress characterization around TSV using *in-situ* PIT-in-SEM," in *Proc. 62nd IEEE Electron. Compon. Technol. Conf. (ECTC)*, May/Jun. 2012, pp. 781–786.

[68] A. Budiman *et al.*, "Measurement of stresses in Cu and Si around through-silicon via by synchrotron X-ray microdiffraction for 3-dimensional integrated circuits," *Microelectron. Rel.*, vol. 52, no. 3, pp. 530–533, Mar. 2012.

[69] M. Stucchi, D. Perry, G. Katti, W. Dehaene, and D. Velenis, "Test structures for characterization of through-silicon vias," *IEEE Trans. Semicond. Manuf.*, vol. 25, no. 3, pp. 355–364, Aug. 2012.

[70] H. S. Kamineni *et al.*, "Challenges to via middle TSV integration at sub-28 nm nodes," in *Proc. IEEE Int. Interconnect Technol. Conf. (IITC)*, May 2014, pp. 199–202.

[71] M. Stucchi, D. Velenis, and G. Katti, "Capacitance measurements of two-dimensional and three-dimensional IC interconnect structures by quasi-static *C–V* technique," *IEEE Trans. Instrum. Meas.*, vol. 61, no. 7, pp. 1979–1990, Jul. 2012.

[72] S. J. Bleiker *et al.*, "High-aspect-ratio through silicon vias for high-frequency application fabricated by magnetic assembly of gold-coated nickel wires," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 5, no. 1, pp. 21–27, Jan. 2015.

[73] J.-M. Yook, D. Kim, J.-C. Park, C.-Y. Kim, S. H. Yi, and J. C. Kim, "Low-loss and high-isolation through silicon via technology for high performance RF applications," in *Proc. 44th Eur. Microw. Conf. (EuMC)*, Oct. 2014, pp. 996–999.

[74] X. Gu *et al.*, "Characterization of TSV-induced loss and substrate noise coupling in advanced three-dimensional CMOS SOI technology," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 3, no. 11, pp. 1917–1925, Nov. 2013.

[75] J. Cho *et al.*, "Modeling and analysis of through-silicon via (TSV) noise coupling and suppression using a guard ring," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 1, no. 2, pp. 220–233, Feb. 2011.

[76] X. Sun *et al.*, "Noise coupling between TSVs and active devices: Planar nMOSFETs vs. nFinFETs," in *Proc. 65th IEEE Electron. Compon. Technol. Conf. (ECTC)*, May 2015, pp. 260–265.

[77] W. Guo *et al.*, "Impact of 3D integration on 7 nm high mobility channel devices operating in the ballistic regime," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2014, pp. 7.1.1–7.1.4.

[78] X. Liu, Q. Chen, V. Sundaram, R. R. Tummala, and S. K. Sitaraman, "Failure analysis of through-silicon vias in free-standing wafer under thermal-shock test," *Microelectron. Rel.*, vol. 53, no. 1, pp. 70–78, Jan. 2013.

[79] A. Mercha *et al.*, "Comprehensive analysis of the impact of single and arrays of through silicon vias induced stress on high-*k*/metal gate CMOS performance," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2010, pp. 2.2.1–2.2.4.

[80] S.-K. Ryu, K.-H. Lu, T. Jiang, J.-H. Im, R. Huang, and P. S. Ho, "Effect of thermal stresses on carrier mobility and keep-out zone around through-silicon vias for 3-D integration," *IEEE Trans. Device Mater. Rel.*, vol. 12, no. 2, pp. 255–262, Jun. 2012.

[81] X. Liu *et al.*, "Reliability assessment of through-silicon vias in multi-die stack packages," *IEEE Trans. Device Mater. Rel.*, vol. 12, no. 2, pp. 263–271, Jun. 2012.

[82] K. H. Lu, X. Zhang, S.-K. Ryu, J. Im, R. Huang, and P. S. Ho, "Thermo-mechanical reliability of 3-D ICs containing through silicon vias," in *Proc. IEEE 59th Electron. Compon. Technol. Conf. (ECTC)*, May 2009, pp. 630–634.

[83] C. Okoro, L. E. Levine, R. Xu, and Y. S. Obeng, "Experimentally, how does Cu TSV diameter influence its stress state?" in *Proc. IEEE 65th Electron. Compon. Technol. Conf. (ECTC)*, May 2015, pp. 54–58.

[84] W. Guo *et al.*, "Copper through silicon via induced keep out zone for 10 nm node bulk FinFET CMOS technology," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2013, pp. 12.8.1–12.8.4.

[85] M. G. Farooq *et al.*, "Impact of 3D copper TSV integration on 32SOI FEOL and BEOL reliability," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2015, pp. 4C.1.1–4C.1.8.

[86] I. De Wolf *et al.*, "Cu pumping in TSVs: Effect of pre-CMP thermal budget," *Microelectron. Rel.*, vol. 51, nos. 9–11, pp. 1856–1859, Sep./Nov. 2011.

[87] J. De Messemaeker *et al.*, "Impact of post-plating anneal and through-silicon via dimensions on Cu pumping," in *Proc. IEEE 63rd Electron. Compon. Technol. Conf. (ECTC)*, May 2013, pp. 586–591.

[88] J. De Messemaeker *et al.*, "Correlation between Cu microstructure and TSV Cu pumping," in *Proc. IEEE 64th Electron. Compon. Technol. Conf. (ECTC)*, May 2014, pp. 613–619.

[89] M. A. Rabie *et al.*, "Novel stress-free keep out zone process development for via middle TSV in 20 nm planar CMOS technology," in *Proc. IEEE Int. Interconnect Technol. Conf. (IITC)*, May 2014, pp. 203–206.

[90] B. Banijamali *et al.*, "Reliability evaluation of an extreme TSV interposer and interconnects for the 20 nm technology CoWoS IC package," in *Proc. 65th IEEE Electron. Compon. Technol. Conf. (ECTC)*, May 2015, pp. 276–280.

[91] N. Tamura *et al.*, "Scanning X-ray microdiffraction with submicrometer white beam for strain/stress and orientation mapping in thin films," *J. Synchrotron Radiat.*, vol. 10, no. 2, pp. 137–143, Mar. 2003.

[92] X. Liu *et al.*, "*In-situ* microscale through-silicon via strain measurements by synchrotron X-ray microdiffraction exploring the physics behind data interpretation," *Appl. Phys. Lett.*, vol. 105, no. 11, pp. 112109-1–112109-5, Sep. 2014.

[93] T. Jiang *et al.*, "Effect of high temperature storage on the stress and reliability of 3D stacked chip," in *Proc. 64th IEEE Electron. Compon. Technol. Conf. (ECTC)*, May 2014, pp. 1122–1127.

[94] P. A. Thadesar and M. S. Bakir, "Novel photo-defined polymer-enhanced through-silicon vias for silicon interposers," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 3, no. 7, pp. 1130–1137, Jul. 2013.

[95] P. A. Thadesar and M. S. Bakir, "Fabrication and characterization of polymer-enhanced TSVs, inductors, and antennas for mixed-signal silicon interposer platforms," *IEEE Trans. Compon., Packag., Manuf. Technol.*, 2016.

[96] Y.-J. Chang *et al.*, "Low slow-wave effect and crosstalk for low-cost ABF-coated TSVs in 3-D IC interposer," in *Proc. 62nd IEEE Electron. Compon. Technol. Conf. (ECTC)*, May/Jun. 2012, pp. 1934–1938.

[97] M. Sunohara, H. Sakaguchi, A. Takano, R. Arai, K. Murayama, and M. Higashi, "Studies on electrical performance and thermal stress of a silicon interposer with TSVs," in *Proc. 60th IEEE Electron. Compon. Technol. Conf. (ECTC)*, Jun. 2010, pp. 1088–1093.

[98] Q. Chen, C. Huang, D. Wu, Z. Tan, and Z. Wang, "Ultralow-capacitance through-silicon vias with annular air-gap insulation layers," *IEEE Trans. Electron Devices*, vol. 60, no. 4, pp. 1421–1426, Apr. 2013.

[99] Y. Civale, M. Gonzalez, D. S. Tezcan, Y. Travaly, P. Soussan, and E. Beyne, "A novel concept for ultra-low capacitance via-last TSV," in *Proc. IEEE Int. Conf. 3D Syst. Integr. (3DIC)*, Nov. 2010, pp. 1–4.

[100] H. Oh, G. S. May, and M. S. Bakir, "Silicon interposer platform with low-loss through-silicon vias using air," in *Proc. IEEE Int. 3D Syst. Integr. Conf. (3DIC)*, Aug./Sep. 2015, pp. TS11.3.1–TS11.3.4.

[101] S.-K. Ryu, K.-H. Lu, X. Zhang, J.-H. Im, P. S. Ho, and R. Huang, "Impact of near-surface thermal stresses on interfacial reliability of through-silicon vias for 3-D interconnects," *IEEE Trans. Device Mater. Rel.*, vol. 11, no. 1, pp. 35–43, Mar. 2011.

[102] Z. Chen, X. Song, and S. Liu, "Thermo-mechanical characterization of copper filled and polymer filled TSVs considering nonlinear material behaviors," in *Proc. 59th IEEE Electron. Compon. Technol. Conf. (ECTC)*, May 2009, pp. 1374–1380.

[103] X. Liu *et al.*, "Dimension and liner dependent thermomechanical strain characterization of through-silicon vias using synchrotron X-ray diffraction," *J. Appl. Phys.*, vol. 114, no. 6, pp. 064908-1–064908-7, Aug. 2013.

[104] P. Thadesar and M. Bakir, "Silicon interposer featuring novel electrical and optical TSVs," in *Proc. ASME Int. Mech. Eng. Congr. Expo. (IMECE)*, Nov. 2012, pp. 405–412.

[105] P. Thadesar and M. Bakir, "Fabrication and characterization of mixed-signal polymer-enhanced silicon interposer featuring photodefined coax TSVs and high-Q inductors," in *Proc. 65th IEEE Electron. Compon. Technol. Conf. (ECTC)*, May 2015, pp. 281–286.

[106] V. Sukumaran *et al.*, "Design, fabrication, and characterization of ultrathin 3-D glass interposers with through-package-vias at same pitch as TSVs in silicon," *IEEE Compon., Packag., Manuf. Technol.*, vol. 4, no. 5, pp. 786–795, May 2014.

[107] B. T. Tung, X. Cheng, N. Watanabe, F. Kato, K. Kikuchi, and M. Aoyagi, "Fabrication and electrical characterization of parylene-HT liner bottom-up copper filled through silicon via (TSV)," in *Proc. IEEE CPMT Symp. Jpn. (ICSJ)*, Nov. 2014, pp. 154–157.

[108] Q. Chen, C. Huang, Z. Tan, and Z. Wang, "Low capacitance through-silicon-vias with uniform benzocyclobutene insulation layers," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 3, no. 5, pp. 724–731, May 2013.

[109] S. W. Ho, S. W. Yoon, Q. Zhou, K. Pasad, V. Kripesh, and J. H. Lau, "High RF performance TSV silicon carrier for high frequency application," in *Proc. 58th IEEE Electron. Compon. Technol. Conf. (ECTC)*, May 2008, pp. 1946–1952.

[110] Q. Chen, Y. Suzuki, G. Kumar, V. Sundaram, and R. R. Tummala, "Modeling, fabrication, and characterization of low-cost and high-performance polycrystalline panel-based silicon interposer with through vias and redistribution layers," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 4, no. 12, pp. 2035–2041, Dec. 2014.

[111] B. Xie, M. Swaminathan, K. J. Han, and J. Xie, "Coupling analysis of through-silicon via (TSV) arrays in silicon interposers for 3D systems," in *Proc. IEEE Int. Symp. Electromagn. Compat. (EMC)*, Aug. 2011, pp. 16–21.

[112] P. A. Thadesar, L. Zheng, and M. S. Bakir, "Low-loss silicon interposer for three-dimensional system integration with embedded microfluidic cooling," in *IEEE Symp. VLSI Technol., Dig. Tech. Papers*, Jun. 2014, pp. 1–2.

[113] T. G. Lim *et al.*, "Through silicon via interposer for millimetre wave applications," in *Proc. 61st IEEE Electron. Compon. Technol. Conf. (ECTC)*, May/Jun. 2011, pp. 577–582.

[114] J.-Y. Lee, S.-W. Lee, S.-K. Lee, and J.-H. Park, "Through-glass copper via using the glass reflow and seedless electroplating processes for wafer-level RF MEMS packaging," *J. Micromech. Microeng.*, vol. 23, no. 8, p. 085012, Aug. 2013.

[115] D. H. Jung *et al.*, "30 Gbps high-speed characterization and channel performance of coaxial through silicon via," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 11, pp. 814–816, Nov. 2014.

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